REMARKS

Claim 25 has been amended. Attached hereto is a marked-up version of the changes made to the claim by the current amendment. The attached page is captioned "Version with markings to show changes made." Claims 25-30 are pending.

Claims 25-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner (U.S. Patent No. 5,899,721) in view of Mogami (U.S. Patent No. 5,656,519). Claims 28-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner in view of Mogami and Bai (U.S. Patent No. 5,861,340). These rejections are respectfully traversed.

The present invention is directed at an integrated circuit. Referring to Figs. 4-9 the semiconductor device of the present invention includes a gate electrode stack 10 disposed upon a dielectric film 16 over a portion of a wafer, such as substrate 17. The gate stack 10 includes a plurality of layers, for example, layers 11, 12, 13, 14, and 15. Above the gate stack 10 is an oxide cap 20. In one embodiment, the electrode stack 10 includes a polysilicon layer 11 and at least one metal layer 13. As shown in the figures, the sidewalls 18 of the electrode stack are continuously vertical. Surrounding the sidewalls 18, continuously from the bottom to the top of the sidewalls 18 are composite spacers, each of which comprise a nitride spacer 22 stacked above an oxide spacer 20. As illustrated, the nitride spacer 22 portion of each composite spacer extends along most of the continuously vertical sidewalls 18, except for the bottom portion. The oxide spacer 22 portion of the composite spacer extends along the bottommost portion of the sidewalls 18. Accordingly,

claim 25 as amended recites an integrated circuit including "a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers located over the gate dielectric film and forms continuously vertical sidewalls; and a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer, said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls."

Gardner is directed at a method of forming small spacers, as illustrated by Fig. 9. Gardner teaches a semiconductor device including a stack, which is comprised of a gate oxide (Fig. 9, layer located immediately under 104), a polysilicon gate conductor 104, and a metal silicide 122. Figs. 3-9 of Gardner illustrate a method of constructing the semiconductor device. Significantly, as illustrated by Fig. 7, Gardner's composite spacer, which comprises a nitride portion 114 and an oxide portion 116, is formed before the stack is fully formed. Indeed, Fig. 7 illustrates the composite spacers as running only along the sidewalls of the stack when the stack consists only of the gate oxide layer and the polysilicon gate conductor layer 104. The metal silicide layer 122 of the stack is not formed until the next step, which is illustrated by Fig. 8, to yield the completed gate stack shown in Fig. 9. As a result of this method of construction, the composite spacers in Gardner's device do not span from the bottom to the top of the sidewalls of the stack. As illustrated in Fig. 9, parts of the sidewall from the metal silicide layer 122 are not

surrounded by the composite sidewall. Gardner therefore fails to disclose or suggest an integrated circuit having "a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers located over the gate dielectric film and forms continuously vertical sidewalls; and a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer, said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls" as required by independent claim 25.

Mogami is directed to a method of manufacturing a MOS device having a salicide gate electrode and source/drain regions. Referring to Fig. 8a, Mogami discloses the formation of a gate electrode stack by depositing: a gate oxide layer 5, a polysilicon layer 6', a tungsten nitride layer 31, and a second polysilicon layer 32. In Fig. 8B, a simple (i.e., single material, or non-composite) oxide spacer 9 is formed which spans the sidewalls of the electrode stack under construction (i.e., layers 5, 6', 31, and 32). In Fig. 8C, the polysilicon layer 32 of the electrode stack under construction (only) is removed, thereby causing the top portion of the oxide spacer 9 to exceed the height of the top portion of the electrode stack under construction (which now has a top at layer 31). In Figs. 8D, 8E, and 8F, a titanium layer is deposited and reacted, then unreacted portions of the titanium layer is removed, and finally a tungsten layer is deposited, respectively. The completed device is illustrated in Fig. 8F, and still retains an oxide sidewall 9 higher than the top of the

electrode stack (now tungsten layer 33). Mogami further discloses that an oxide space which exceeds the height of the electrode stack is advantageous for preventing short circuits. Column 8, lines 5-15.

The Office Action asserts that the teachings of Gardner and Mogami can be combined to result in the claimed invention and would advantageously share the same resistance to short circuits as taught by Mogami. However, if the technique of Mogami were incorporated into that of Gardner, an additional polysilicon layer would needed to be deposited on the electrode stack and subsequently removed, since that is the mechanism used by Mogami at Fig. 8C to produce its oxide sidewall. Assuming such a technique were incorporated into the process disclosed by Gardner, there would be no need for a nitride space since the oxide space would extend beyond the top of the sidewall, and the resulting device would not have a composite space formed from a nitride space stacked upon an oxide spacer, as required by claim 25. Alternatively, even if an nitride were formed, the resulting device would not have "a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers located over the gate dielectric film and forms continuously vertical sidewalls; and a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer, said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls" as required by amended claim 25.

Bai is cited by the Office Action for teaching a refractory silicide metal layer, a diffusion layer, and a barrier layer which is substantially impermeable to silicon and metal atoms. However, Bai does not teach or suggest the gate electrode stack and composite spacer of the invention.

The cited prior art is devoid of any teachings or suggestions regarding "a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers located over the gate dielectric film and forms continuously vertical sidewalls; and a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer, said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls." Claim 25 is therefore believed to be allowable over the prior art of record.

Claims 26-30 depend from claim 25 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: October 15, 2002

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant

Version With Markings to Show Changes Made

Please amend claim 25 as follows:

25. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric film disposed on a surface of the substrate;

a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers located over the gate dielectric film and forms [forming] continuously vertical sidewalls; and

a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls,

wherein

each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer,[.]

said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and

said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls.